


LCFC NM-C821

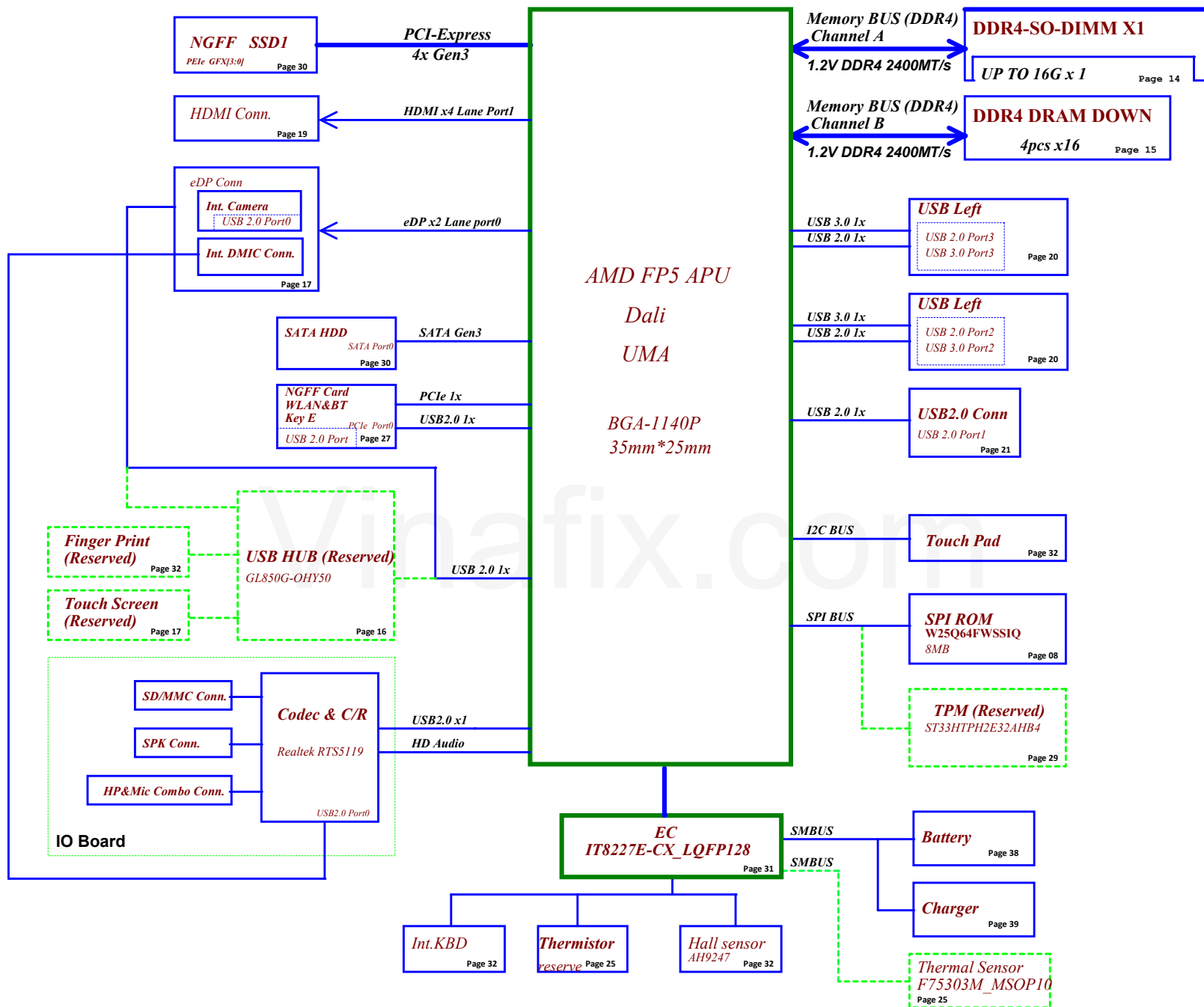
M/B Schematics Document

AMD FP5 DALI SOC with DDRIV

2019-12-05

REV:1.0

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2013/08/15	Deciphered Date	2013/08/15	Cover Page			
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				Custom	S350 ADA	1.0	
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<div>power plane</div> <div>State</div>	<div>B+ (+20VSB)</div> <div>+3VL</div> <div>+5VLP</div>	<div>+5VALW</div> <div>+3VALW (+3VALW_APU)</div> <div>+1.8VALW</div> <div>+0.9VALW</div>	<div>+1.2V</div>	<div>+5VS</div> <div>+3VS</div> <div>+1.8VS</div> <div>+0.9VS</div> <div>+0.6VS</div> <div>+2.5VS</div> <div>+VDDC_VDD</div> <div>+VDDCR_SOC</div> <div>+VDDC</div> <div>+VDDCI</div> <div>+3VGS</div> <div>+1.8VGS</div> <div>+1.35VGS</div>
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF	OFF

	SOURCE	Device
TP_I2C0_SCL	APU	Touch Pad
TP_I2C0_SDA	+3VALW	+3VS

Device	Address
Elan: SA469D-22HA 69x104x1.0	?
Synaptics: TM-P3255-008 69x104x1.0	?

[illegible]


Device	Address	Device	Address	Device
Battery	?	PMIC	0X34	GPU
Charger	0001 0010 b	Thermal Sensor	1001_100xb(reserve)	APU SB-TSI

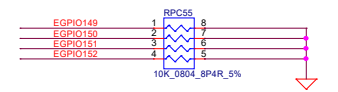
Device	Address	Device
PMIC	0X34	GPU
Thermal Sensor	1001_100xb(reserve)	APU SB-TSI

Device	Address
GPU	0x41(default)
APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting

Device	Address
DDR4 SO-DIMM	?
WLAN	RSVD

HSIO Port		Device
GPP	0	WLAN
	1	N/A
	2	N/A
	3	N/A
	4	N/A
	5	N/A
	6	HDD
	7	
GFX	0	
	1	
	2	
	3	
	4	
	5	N/A
	6	
	7	
USB3.0	0	N/A
	1	N/A
	2	LEFT USB (3.0) lower
	3	LEFT USB (3.0) upper
	4	N/A
USB2.0	0	CardReader
	1	USB2.0
	2	LEFT USB (3.0) lower
	3	LEFT USB (3.0) upper
	4	USB HUB
	5	BT

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PSA_I2C_SCL RC3126 2 1 4.7K 0402 5%
PSA_I2C_SDA RC3127 2 1 4.7K 0402 5%

I2C2_SCL_APU 3 2
I2C2_SDA_APU 2 1

2.2K 0404 4P2R_5%

+3VS_APU

EC_SMI# RC3081 1 2 2.2K 0402 5%
PCR_TP_INT# RC3213 1 2 10K 0402 5%
APU_SSD_RST# RC3246 1 2 10K 0402 5%

TP12C0_SDA_RA 3
TP12C0_SCL_RA 4

2.2K 0404 4P2R_5%

PB1TN_OUT# 1
PC1E_WAKEUP_RA 2
AC_PRESENT 3

10K 0804 8P4R_5%

Blink
PM_SLP_SS#
PM_SLP_SS#
AP0_SLD_RST#

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

2.2K 0402 5%
2.2K 0402 5%
2.2K 0402 5%
2.2K 0402 5%

+3VALW_AP

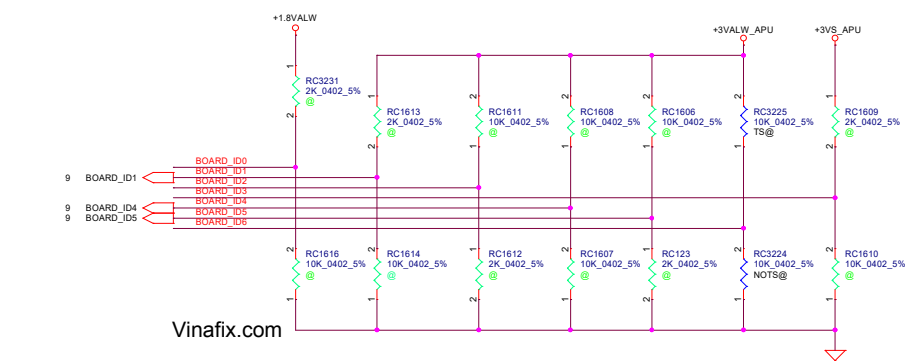
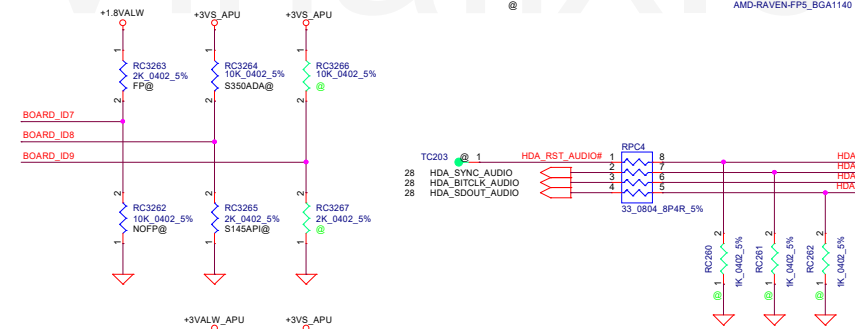
Signal	Pin	Value	Unit	Frequency	Amplitude
PCH_TP_INT#	RC248	1	2	10K	0402 5%
RSMRST#_R	RC87	1	2	100K	0402 5%
SYS_PWRGD_R	RC89	1	2	100K	0402 5%
PCIE_RST#_R	RC3227	1	2	10K	0402 5%

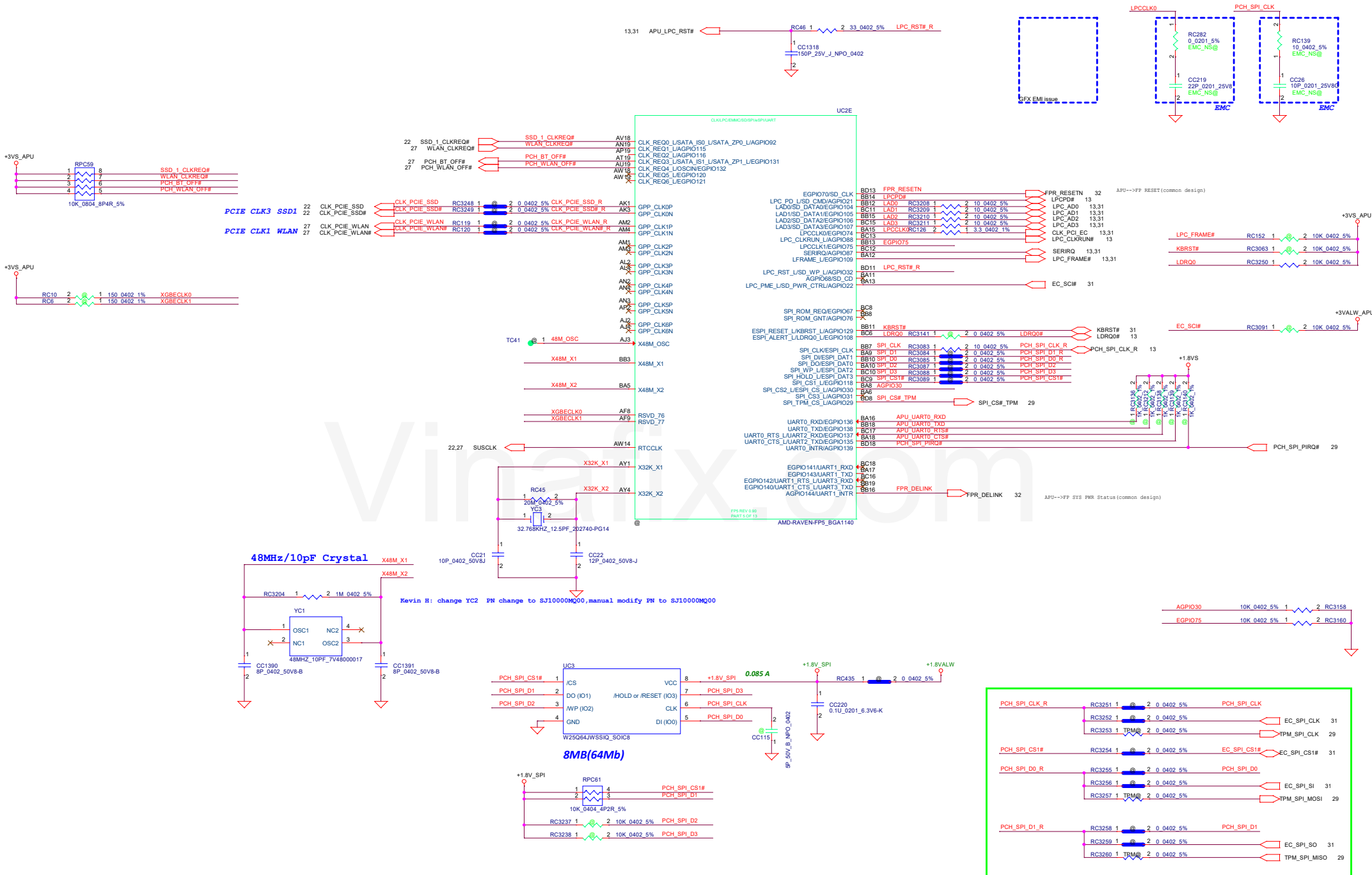
PM_SLP_S3#CC8791 10 2 4700P 25V K X7R 0201
PM_SLP_S5#CC8792 10 2 4700P 25V K X7R 0201

SDOUT

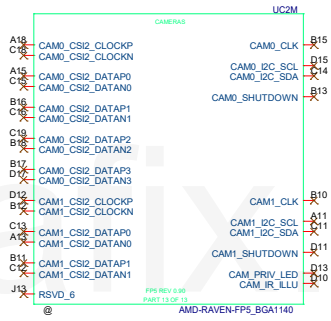
FP5 AZ/I2C/ACPI/GPIO

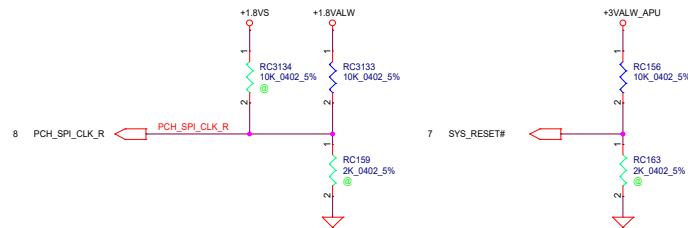
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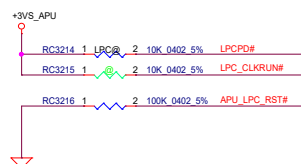
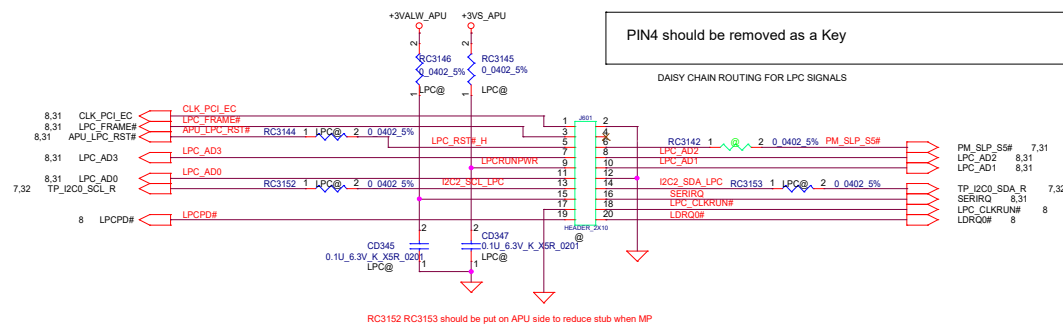
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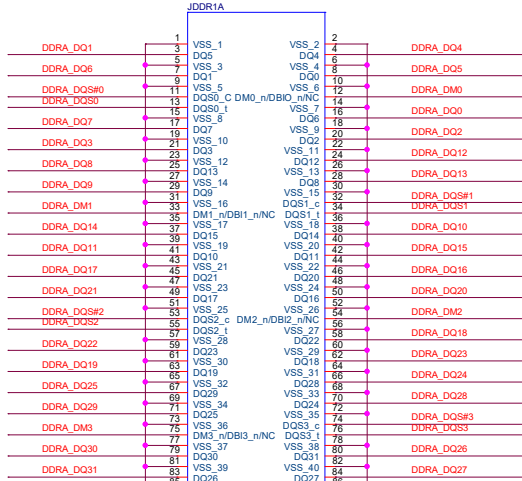


STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE (DEFAULT) 0:SHORT RESET MODE

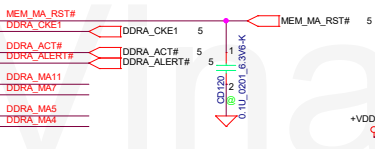
LPC ROM EMULATOR HEADER



update JDDR1 symbol 1129

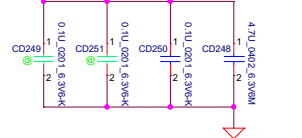


for MEM_MB_RST# overshoot issue

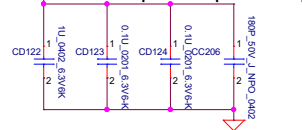


Layout Note: Place near JDDR1

follow CRB 1pcs 4.7uf + 1pcs 0.1uf

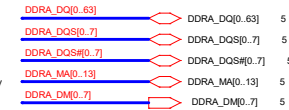
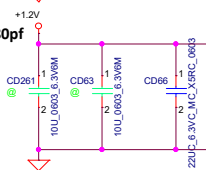
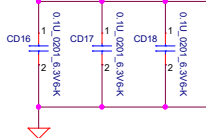


follow CRB 1pcs 1uf + 2pcs 0.1uf + 1pcs 180pf



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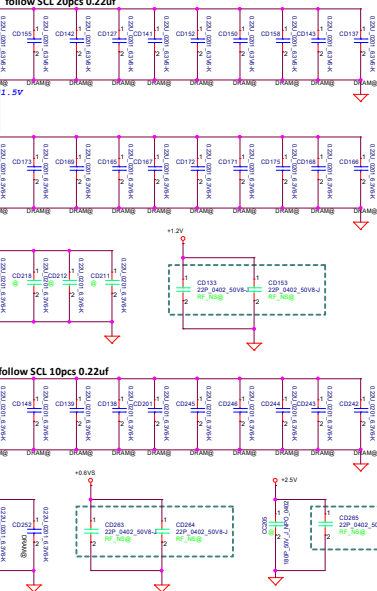
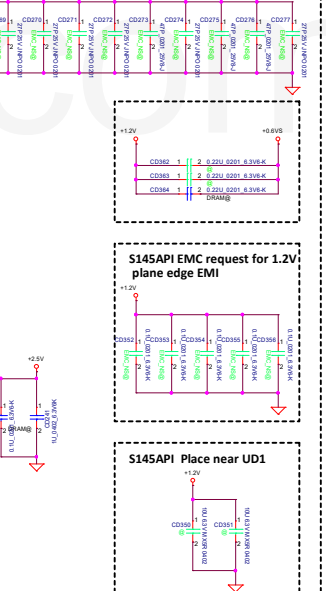
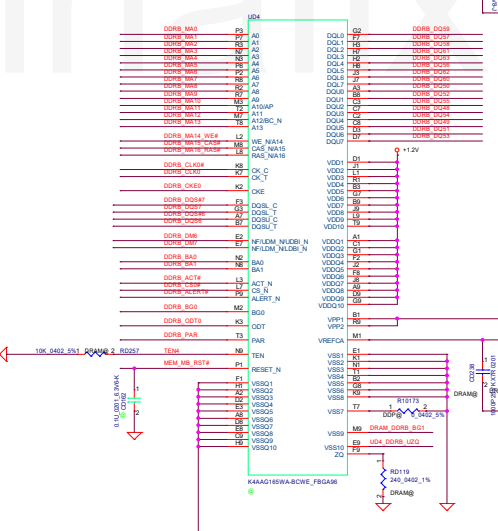
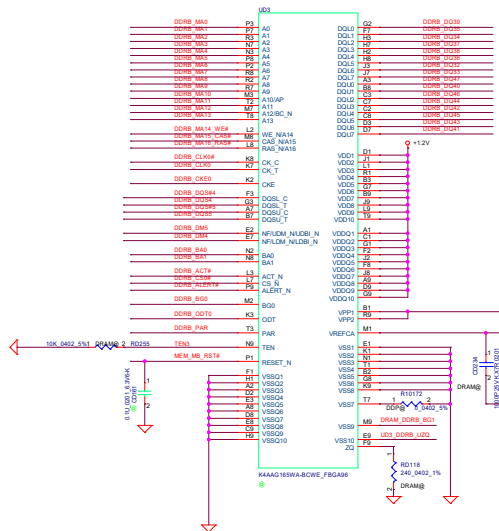
follow CRB 6pcs 0.1uf



Swap Table

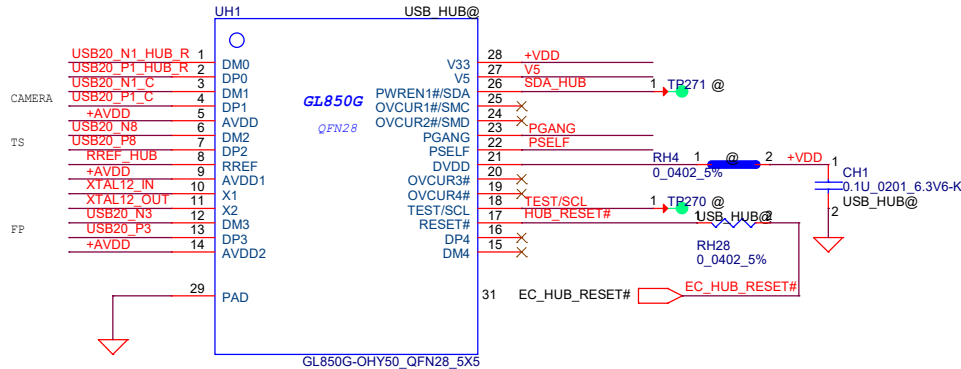
Pin Name	Net Name
DQ0	DDR_A_DQ6
DQ1	DDR_A_DQ5
DQ2	DDR_A_DQ4
DQ3	DDR_A_DQ3
DQ4	DDR_A_DQ2
DQ5	DDR_A_DQ1
DQ6	DDR_A_DQ0
DQ7	DDR_A_DQ7
DQ8	DDR_A_DQ8
DQ9	DDR_A_DQ9
DQ10	DDR_A_DQ10
DQ11	DDR_A_DQ11
DQ12	DDR_A_DQ12
DQ13	DDR_A_DQ13
DQ14	DDR_A_DQ14
DQ15	DDR_A_DQ15
DQ16	DDR_A_DQ16
DQ17	DDR_A_DQ17
DQ18	DDR_A_DQ18
DQ19	DDR_A_DQ19
DQ20	DDR_A_DQ20
DQ21	DDR_A_DQ21
DQ22	DDR_A_DQ22
DQ23	DDR_A_DQ23
DQ24	DDR_A_DQ24
DQ25	DDR_A_DQ25
DQ26	DDR_A_DQ26
DQ27	DDR_A_DQ27
DQ28	DDR_A_DQ28
DQ29	DDR_A_DQ29
DQ30	DDR_A_DQ30
DQ31	DDR_A_DQ31
DQ32	DDR_A_DQ32
DQ33	DDR_A_DQ33
DQ34	DDR_A_DQ34
DQ35	DDR_A_DQ35
DQ36	DDR_A_DQ36
DQ37	DDR_A_DQ37
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DQ41	DDR_A_DQ41
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DQ66	DDR_A_DQ66
DQ67	DDR_A_DQ67
DQ68	DDR_A_DQ68
DQ69	DDR_A_DQ69
DQ70	DDR_A_DQ70
DQ71	DDR_A_DQ71
DQ72	DDR_A_DQ72
DQ73	DDR_A_DQ73
DQ74	DDR_A_DQ74
DQ75	DDR_A_DQ75
DQ76	DDR_A_DQ76
DQ77	DDR_A_DQ77
DQ78	DDR_A_DQ78
DQ79	DDR_A_DQ79
DQ80	DDR_A_DQ80

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SPD Address = A2H

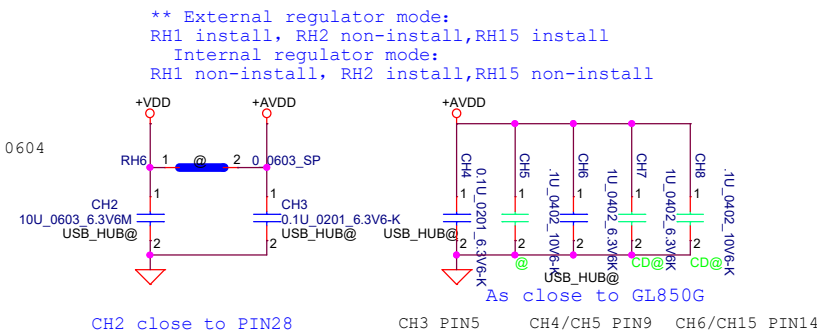
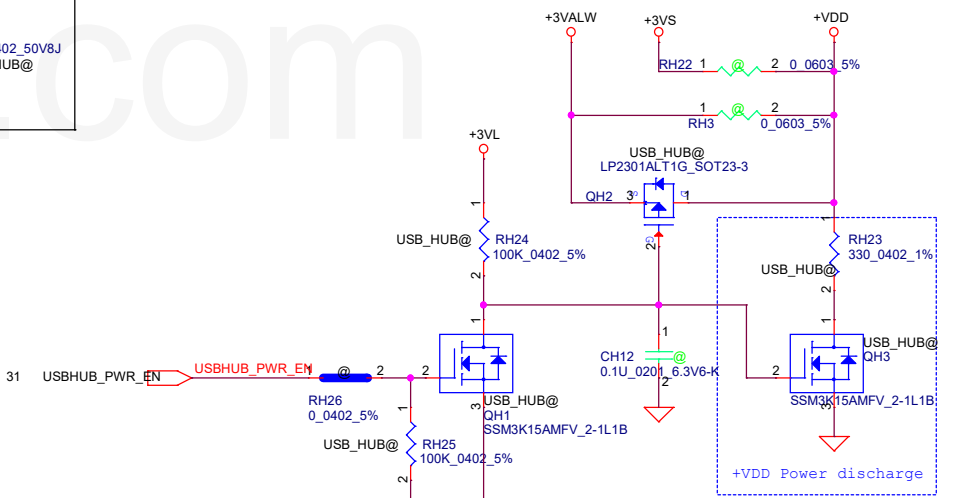
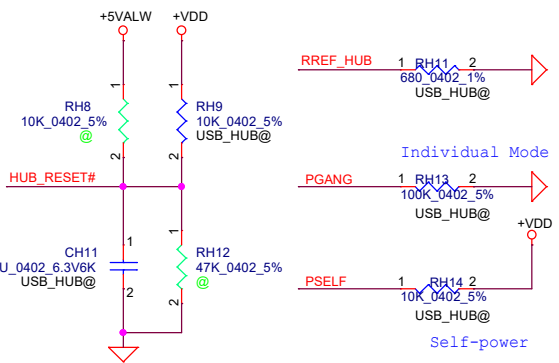
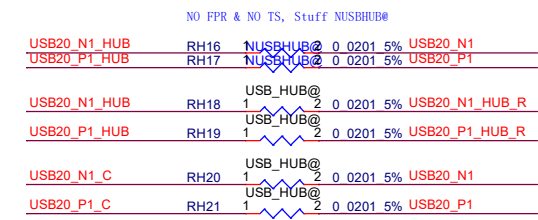
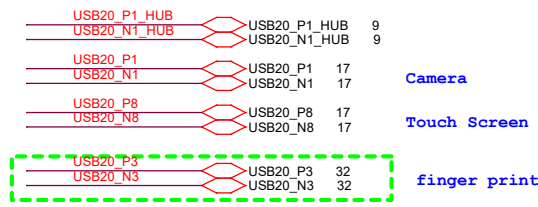
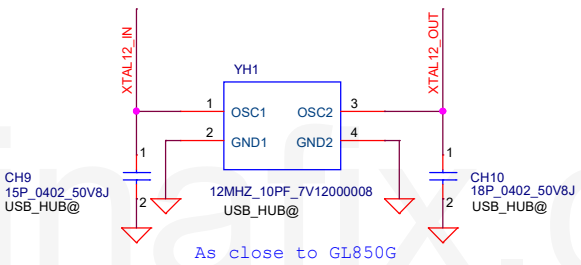


Pin Name	Net Name
D08	D08_D03
D09	D08_D04
D02	D08_D02
D03	D08_D03
D04	D08_D04
D05	D08_D05
D06	D08_D06
D07	D08_D07
D08	D08_D08
D09#0	D08_D09#0
UD1	
D08	D08_D08
D09	D08_D09
D10	D08_D10
D11	D08_D11
D12	D08_D12
D13	D08_D13
D14	D08_D14
D15	D08_D15
D08#1	D08_D08#1
UD1	
D07	D08_D07
D17	D08_D17
D18	D08_D18
D19	D08_D19
D20	D08_D20
D21	D08_D21
D22	D08_D22
D23	D08_D23
D08#2	D08_D08#2
D09#1	D08_D09#1
UD2	
D24	D08_D24
D25	D08_D25
D26	D08_D26
D27	D08_D27
D28	D08_D28
D29	D08_D29
D30	D08_D30
D31	D08_D31
D08#3	D08_D08#3
D09#2	D08_D09#2
UD2	
D32	D08_D32
D33	D08_D33
D34	D08_D34
D35	D08_D35
D36	D08_D36
D37	D08_D37
D38	D08_D38
D39	D08_D39
D40#4	D08_D40#4
D41	D08_D41
UD3	
D42	D08_D42
D43	D08_D43
D44	D08_D44
D45	D08_D45
D46	D08_D46
D47	D08_D47
D48	D08_D48
D49	D08_D49
D50	D08_D50
D51	D08_D51
D52	D08_D52
D53	D08_D53
D54	D08_D54
D55	D08_D55
D08#5	D08_D08#5
D09#3	D08_D09#3
UD4	
D56	D08_D56
D57	D08_D57
D58	D08_D58
D59	D08_D59
D60	D08_D60
D61	D08_D61
D62	D08_D62
D63	D08_D63
D64	D08_D64
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D67	D08_D67
D68	D08_D68
D69	D08_D69
UD4	

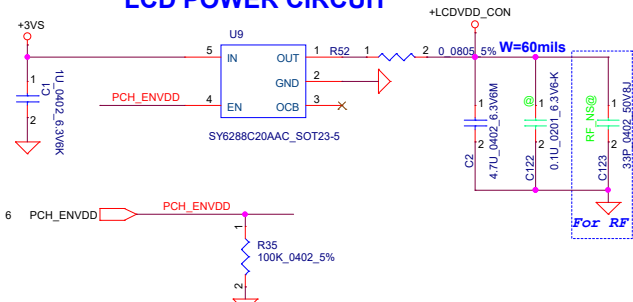
for USB HUB update to OHY50, manual modify PN to GL850G-OHY50



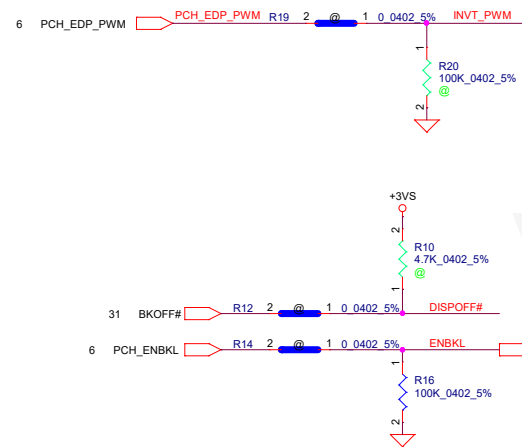
PORT1	Camera
PORT2	Touch Screen
PORT3	Finger print



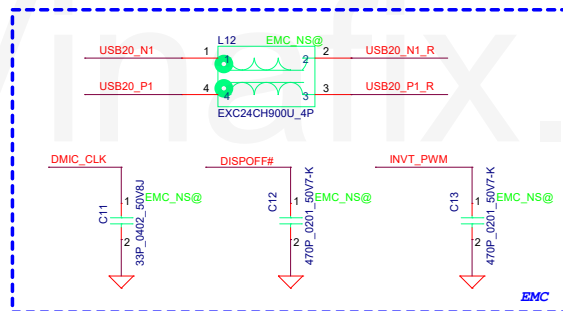
LCD POWER CIRCUIT



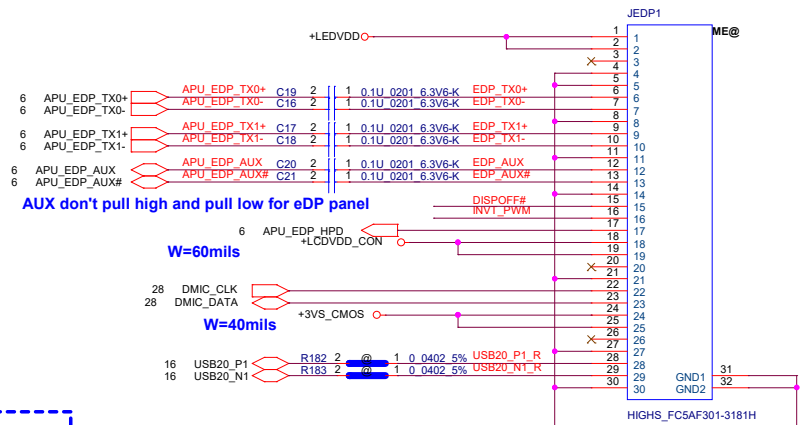
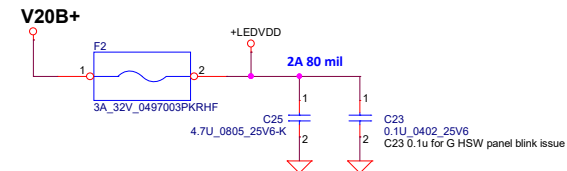
APU output enable Voh min is 1.8V-0.45V=1.35V



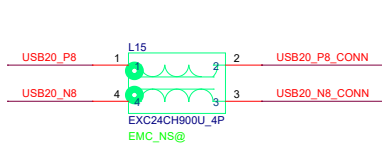
CMOS Camera



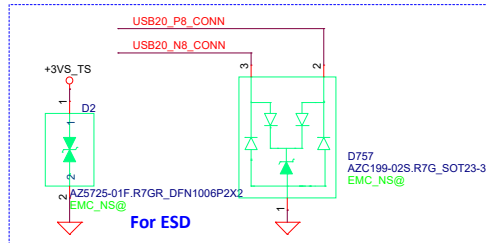
B+ to +LEDVDD POWER



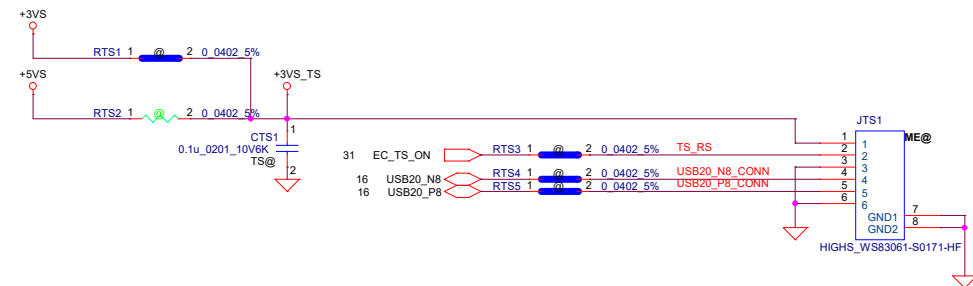
Touch Screen



For EMI

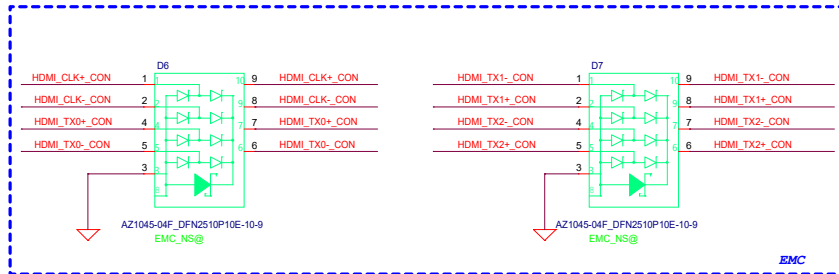
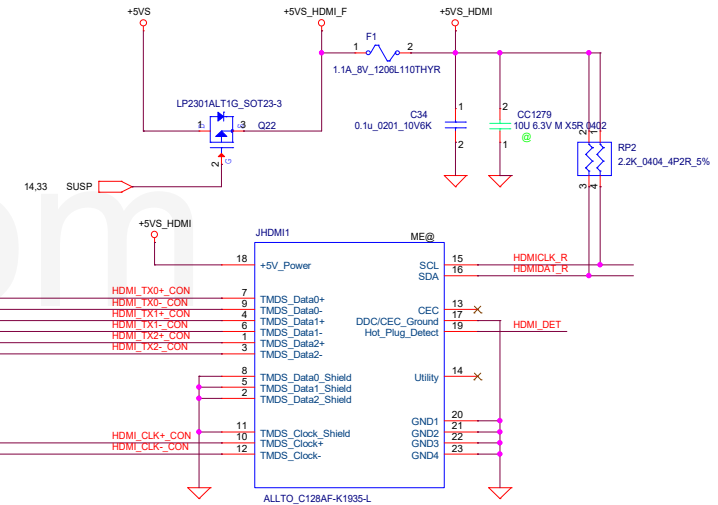
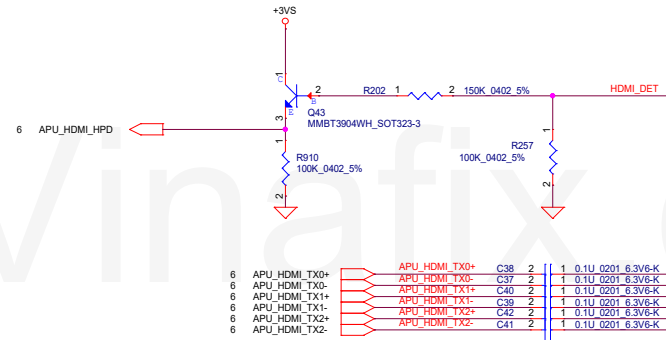
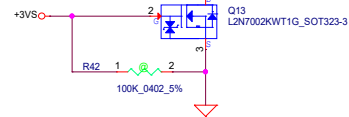
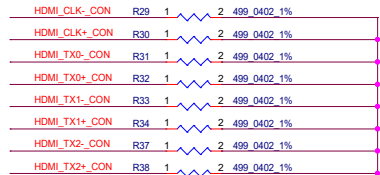
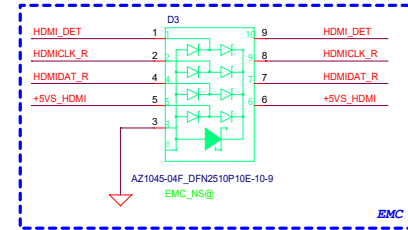
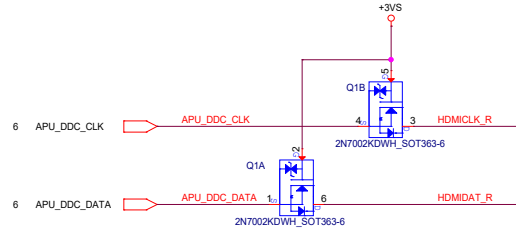
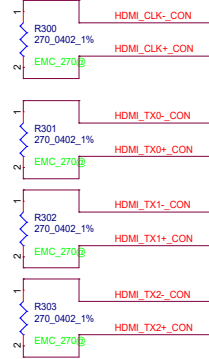


For ESD

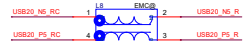
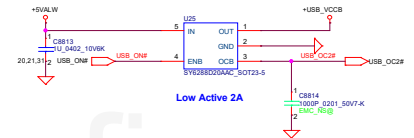
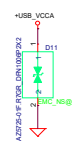
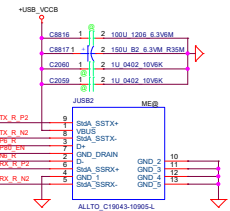


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7/29 S145API EMC request for HDMI

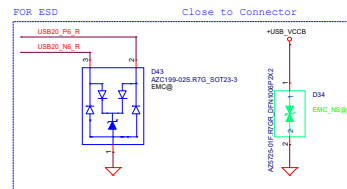


Security Classification		LC Future Center Secret Data		Title	
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				Sheet	19 of 44

[illegible][illegible][illegible]

Pin connection diagram for the NCY3958Y module. The module is labeled U129 and NCY3958Y. The connections are as follows:

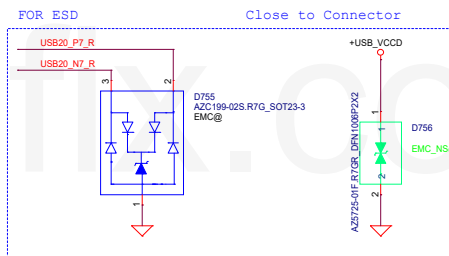
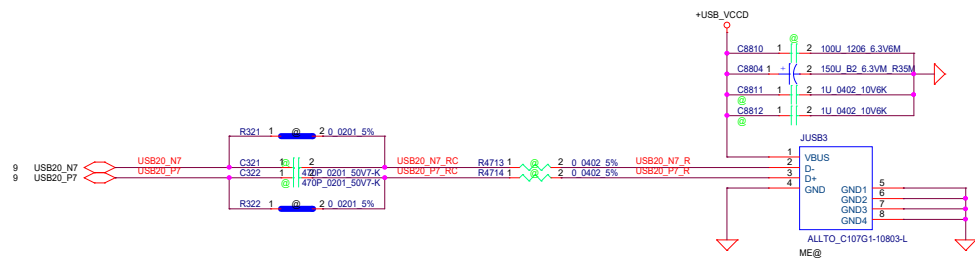
- Pin 1: EC_TX, connected to R533 2 0402 1 0 0402 5% EC_TX C 1
- Pin 2: EC_RX, connected to R536 2 0402 1 0 0402 5% EC_RX C 2
- Pin 3: USB20_PN, connected to D+
- Pin 4: USB20_NE, connected to D-
- Pin 5: GND1, connected to GND
- Pin 6: GND2, connected to GND
- Pin 7: VCC, connected to VCC
- Pin 8: D+, connected to D+
- Pin 9: D-, connected to D-
- Pin 10: D+, connected to D+
- Pin 11: D-, connected to D-

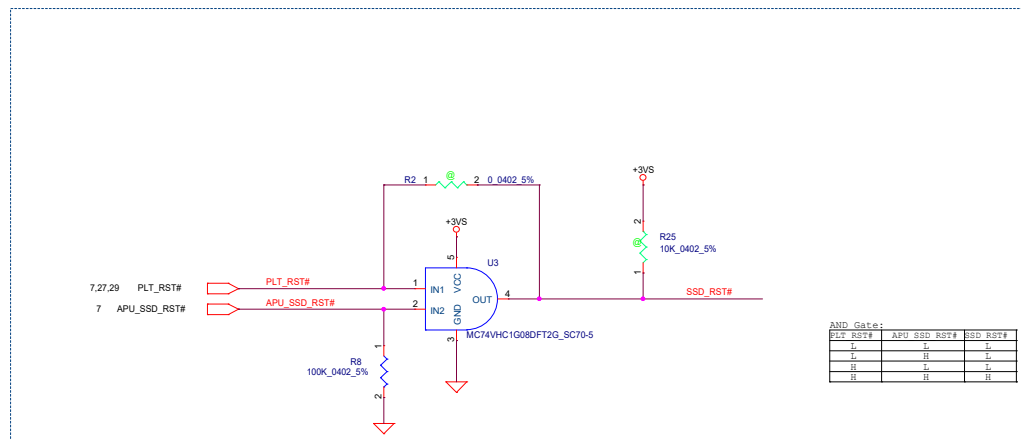
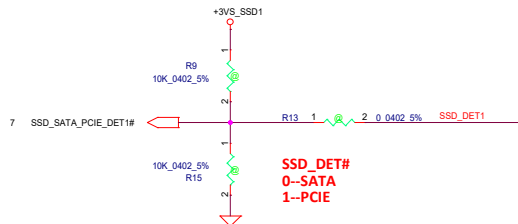
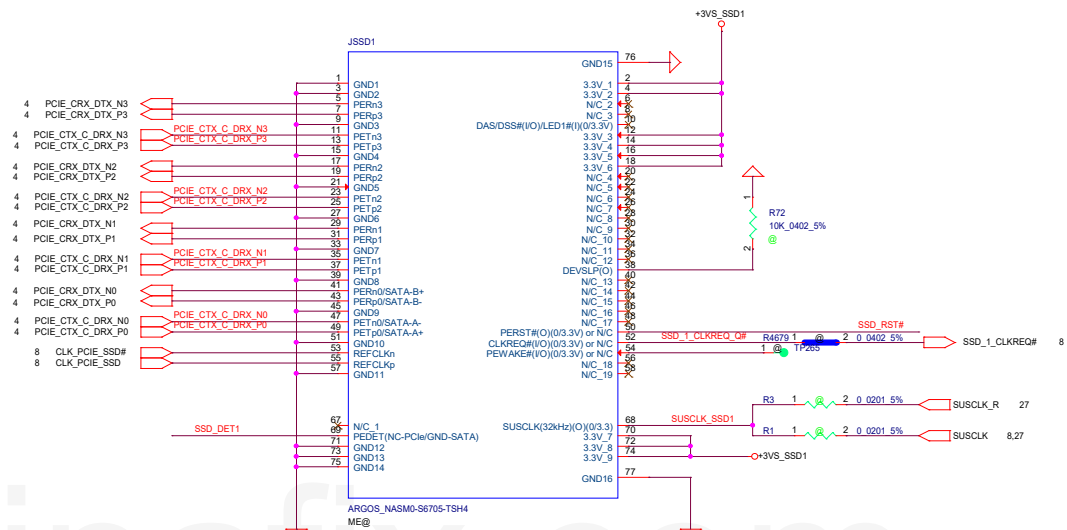
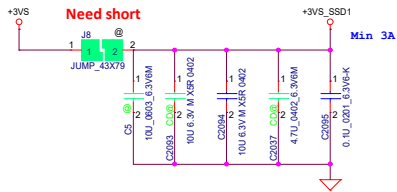


OE#	S	FUNCTION
W	X	DISABLE
L	L	D(+/=) to 1D(+/=)
L	H	D(+/=) to 2D(+/=)

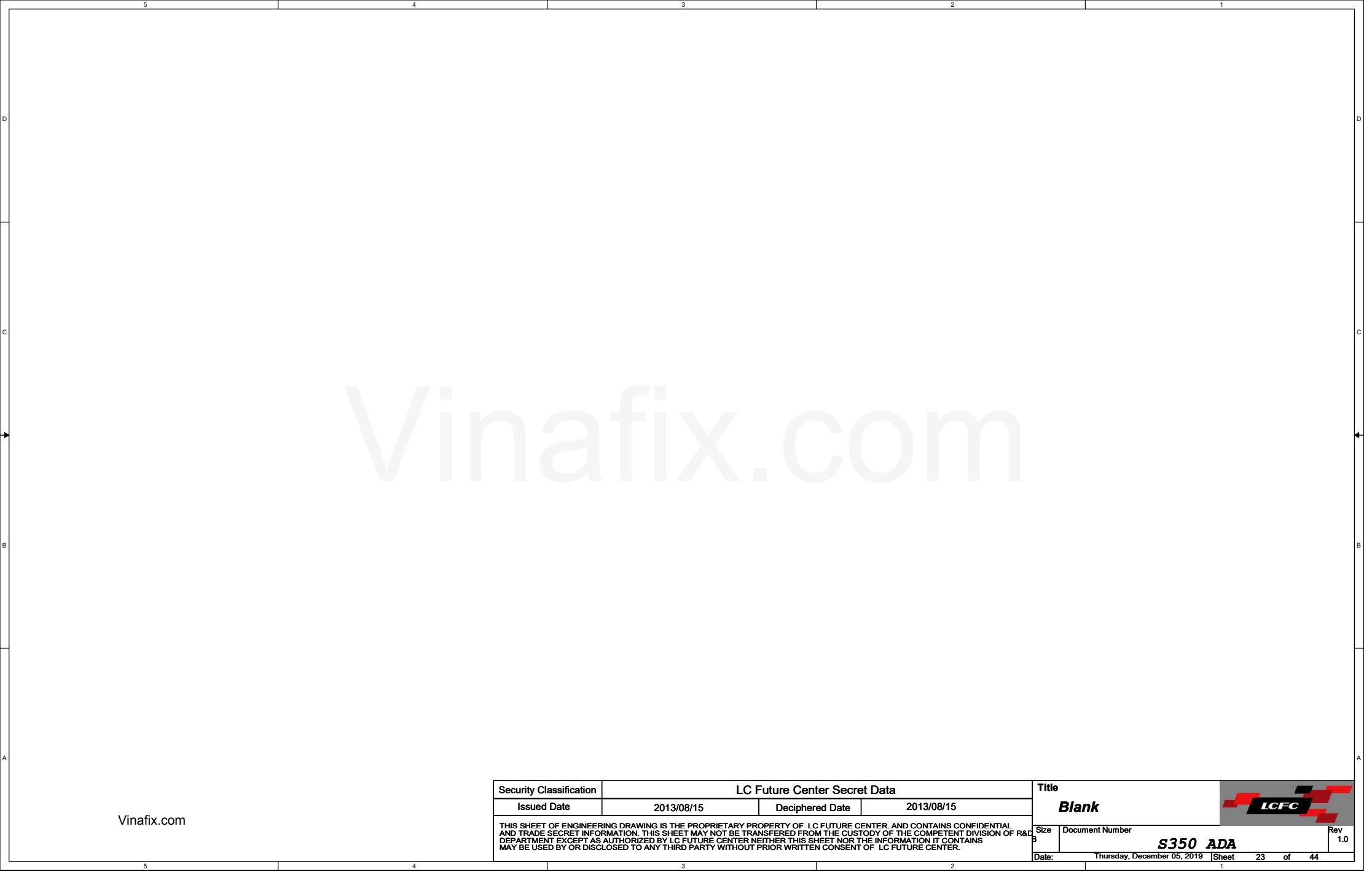
Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	

Title		
USB3.0 PORT (LEFT)		
Size	Document Number	Rev
Custom	S350 ADA	1.0






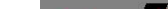
PLT_RST#	APU_SSD_RST#	SSD_RST#
I	I	I
I	I	I
I	I	I
I	I	I



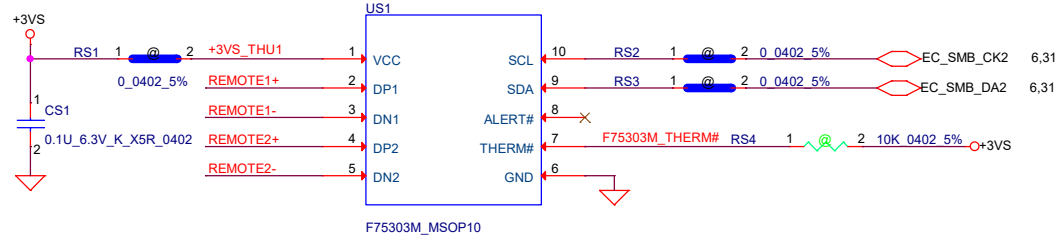
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				Date:	Thursday, December 05, 2019	Rev 1.0 Sheet 24 of 44

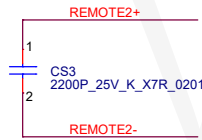
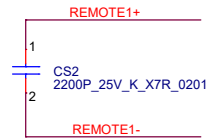
Thermal Sensor placed nearby SO-DIMM



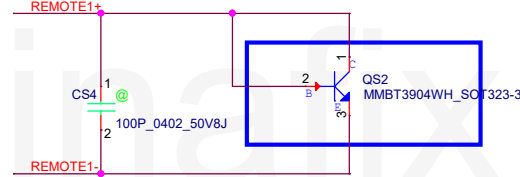
Address 1001_101xb
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

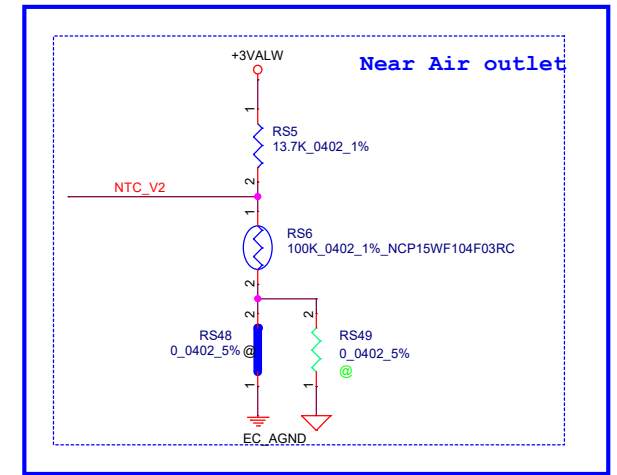
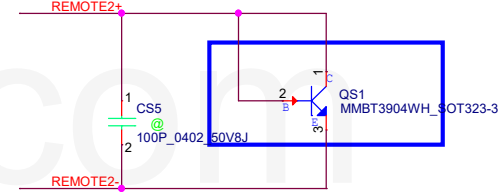
Close to US1



Close to Charger

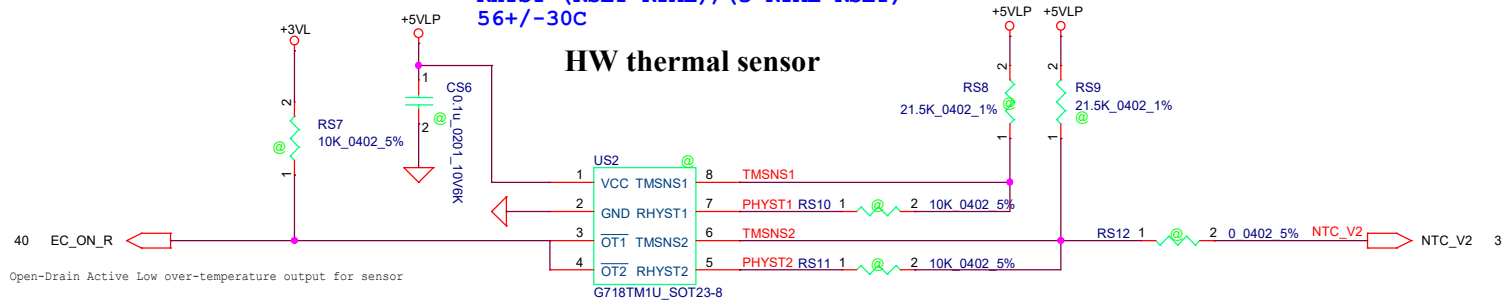


Close APU



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML) / (3*RTML-RSET)
56+/-30C

HW thermal sensor

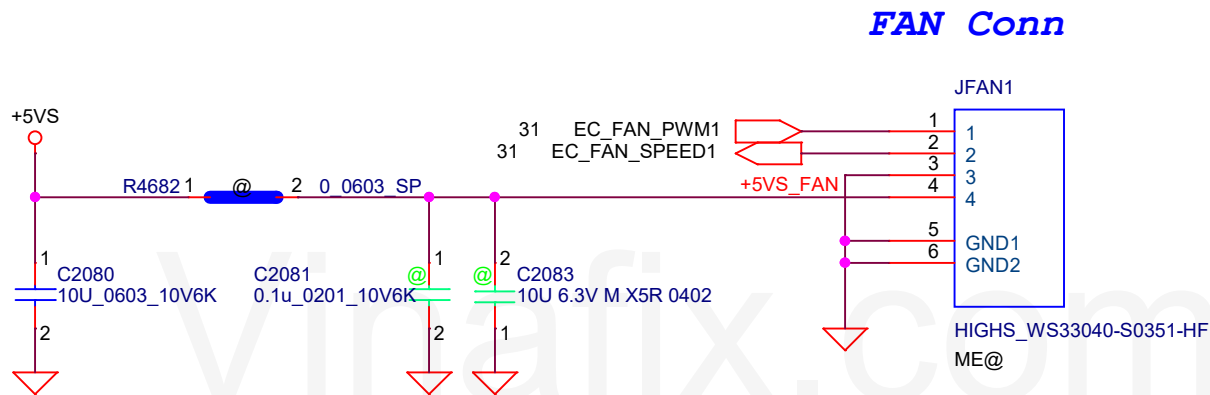



Open-Drain Active Low over-temperature output for sensor

Vinafix

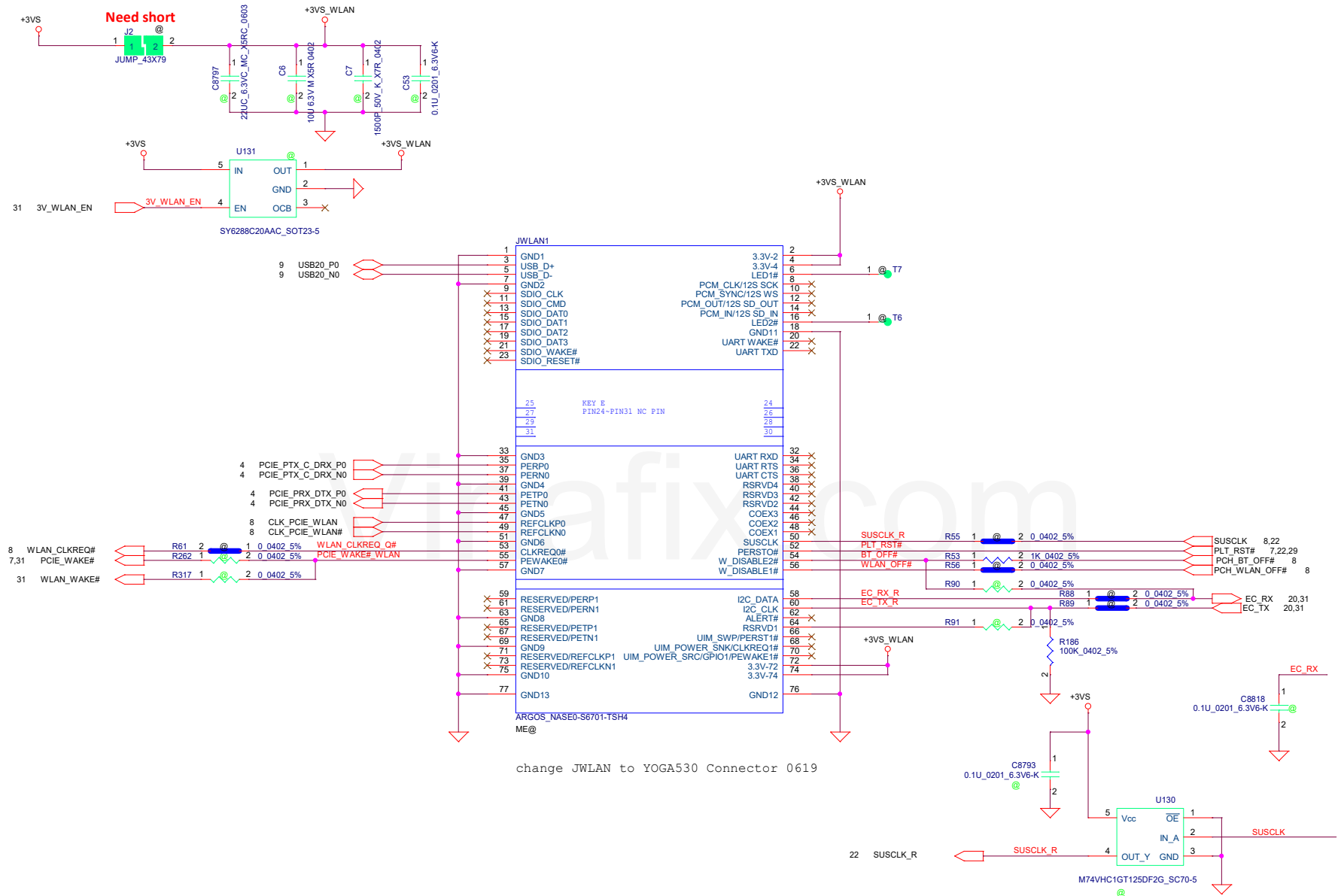
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Rev		1.0			

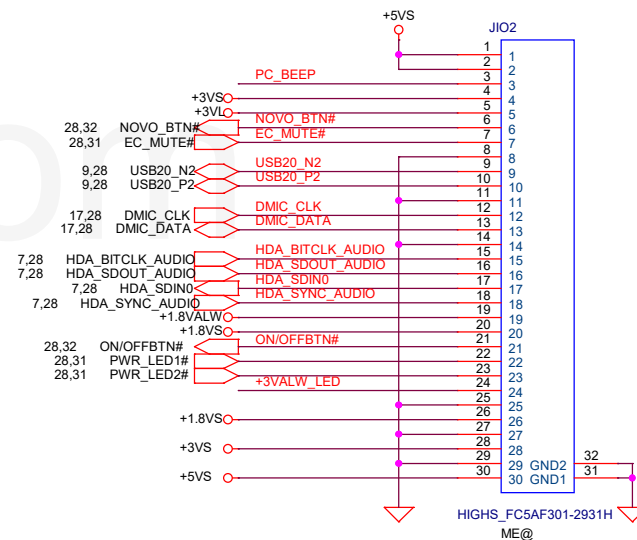
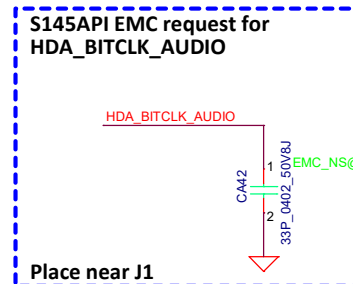


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Mini-Express Card(WLAN/WiMAX)




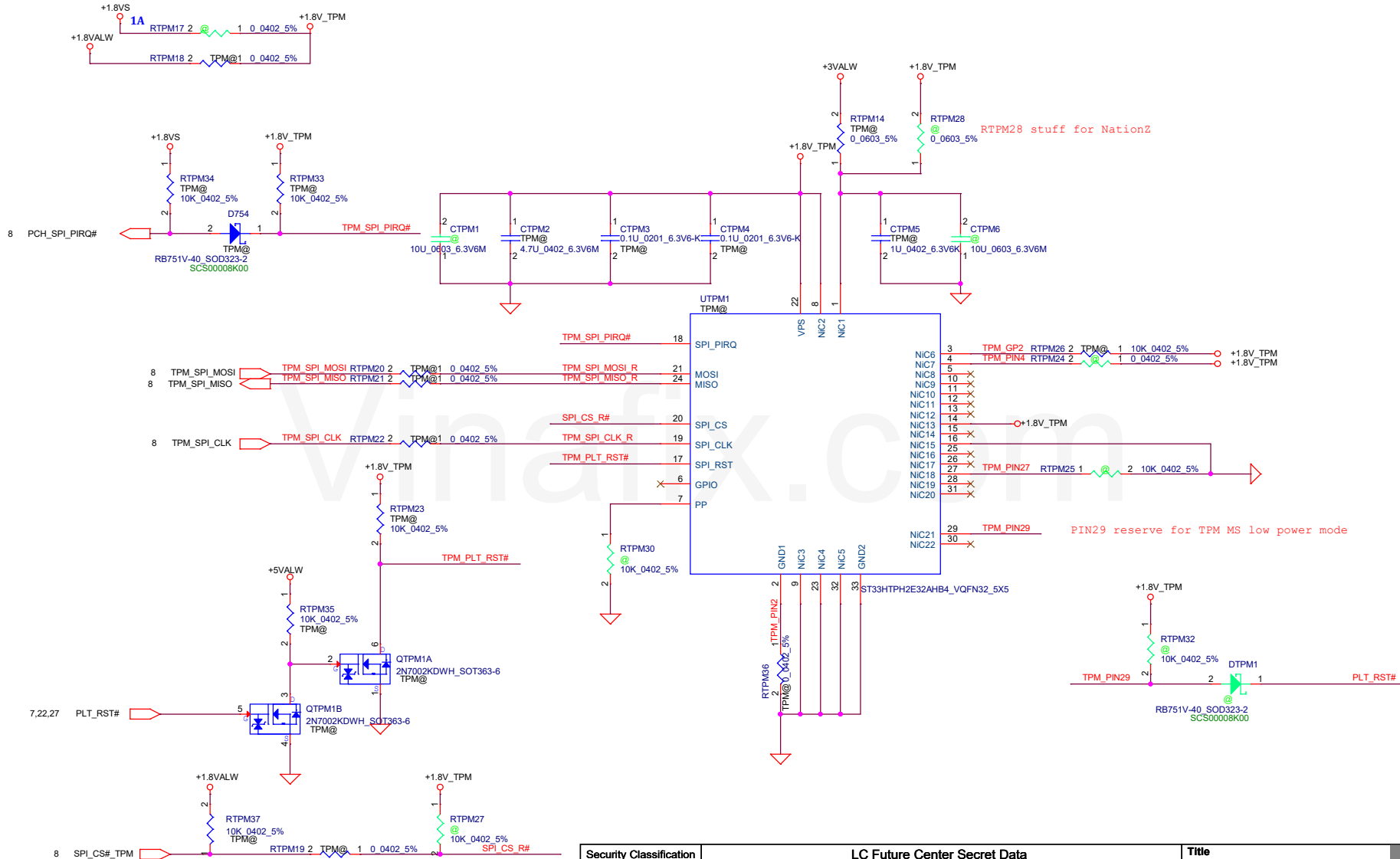
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change SP01001IF00 to SP01001YP00(30pin)0619

30Pin CONN

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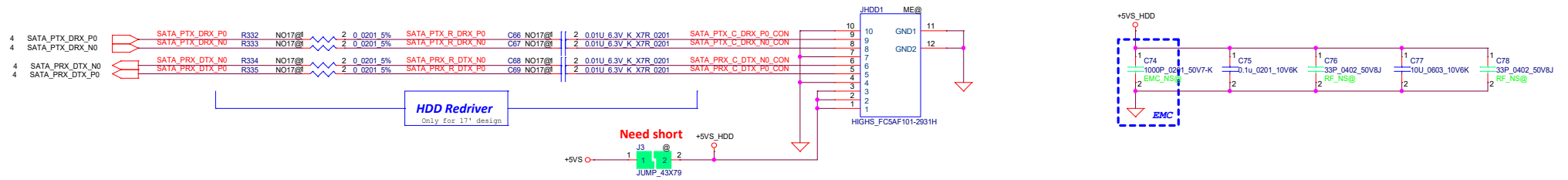
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						Custom		S350 ADA		1.0	
						Date		Thursday, December 05, 2019		Sheet 29 of 44	

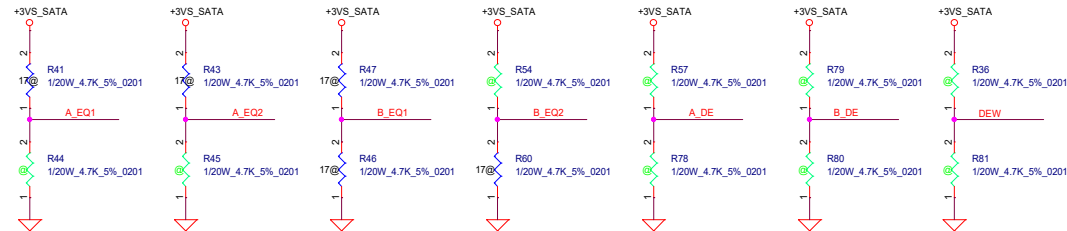
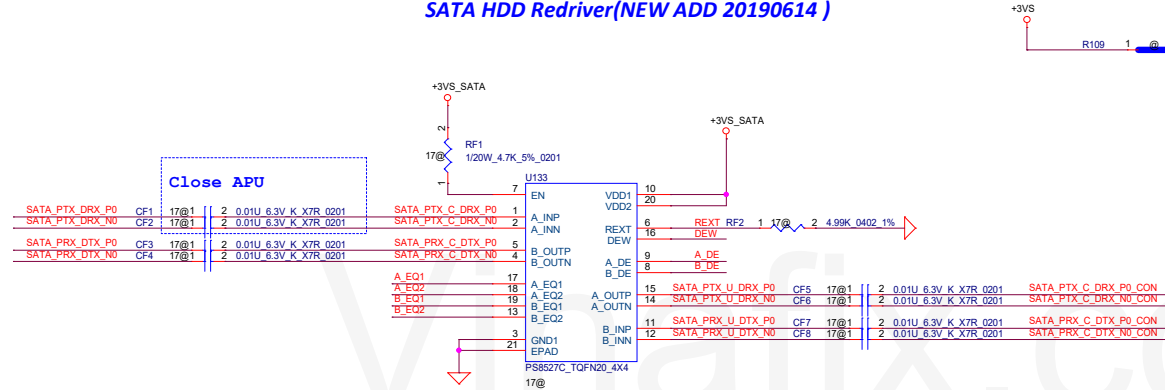


Rrev 1.0

SATA HDD Conn.



SATA HDD Redriver(NEW ADD 20190614)



Equalization level setting for Channel x(x=A/B), internally tied to VDD/2

[x_EO2, x_EO1] ==

- L/M: for channel loss up to 2.4dB
- L/L: for channel loss up to 7.4dB
- L/H: for channel loss up to 14.4dB
- M/M: for channel loss up to 12.2dB (default)
- M/L: for channel loss up to 9.4dB
- M/H: for channel loss up to 13.3dB
- H/M: for channel loss up to 6.2dB
- H/L: for channel loss up to 11.2dB
- H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally pulled down

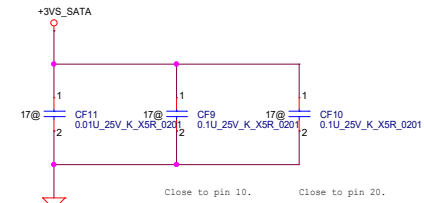
[x_DE] ==

- M: -3.5dB (default)
- L: 0dB
- H: -6dB

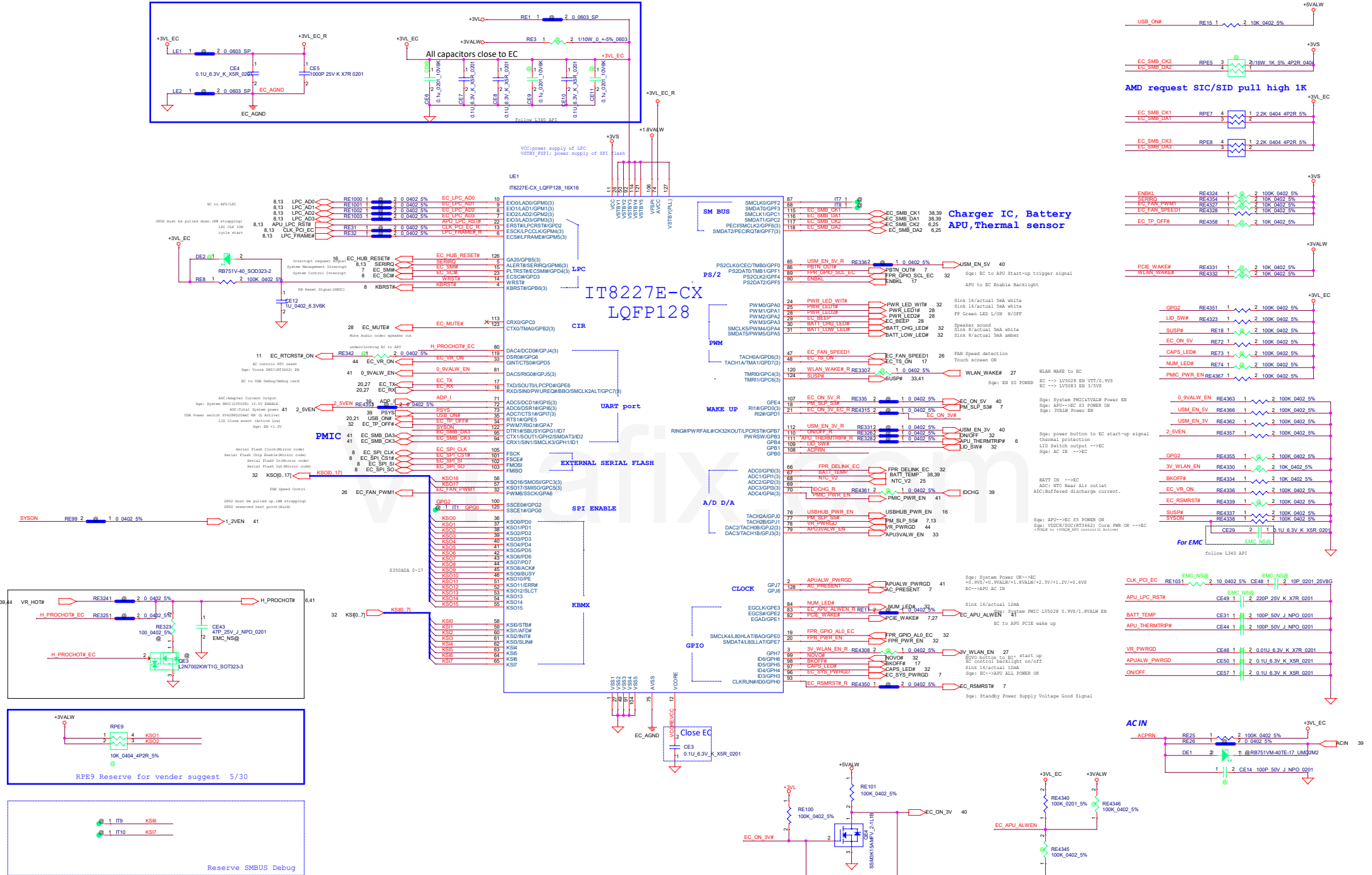
De-emphasis width adjustment, internally pulled down

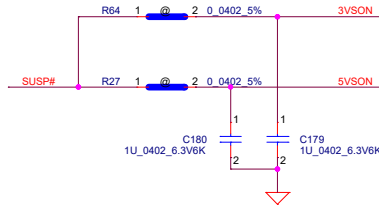
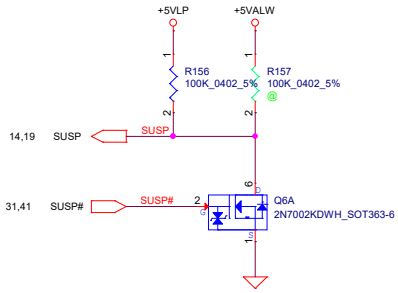
[DEW] ==

- M: for SATA3 (default)
- L: for SATA3
- H: for SATA2



Follow Vendor suggest

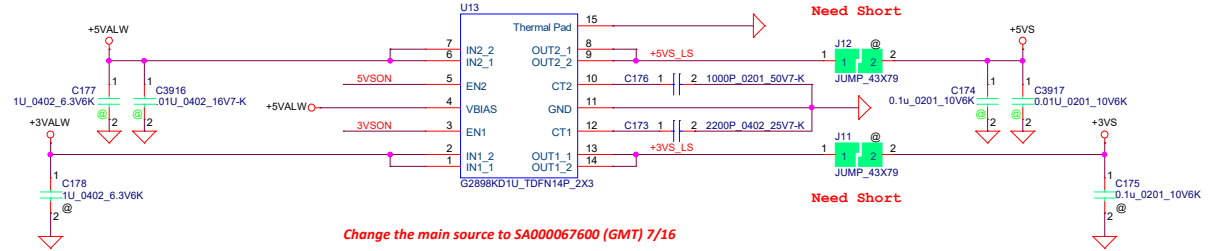




Load Switch
+5VALW To +5VS
+3VALW To +3VS

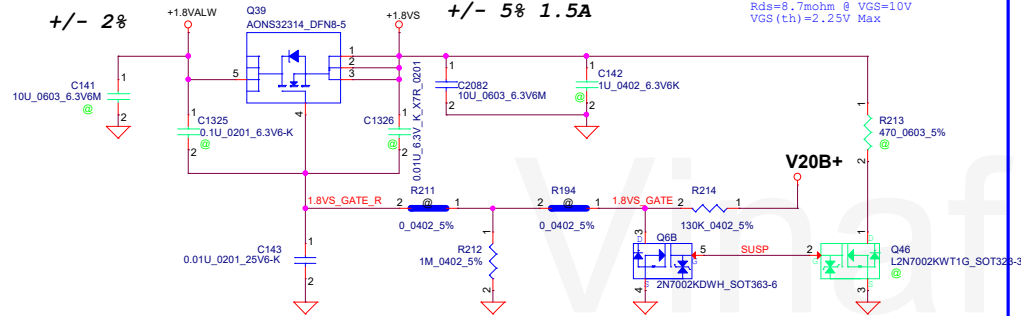
+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



Change the main source to SA000067600 (GMT) 7/16

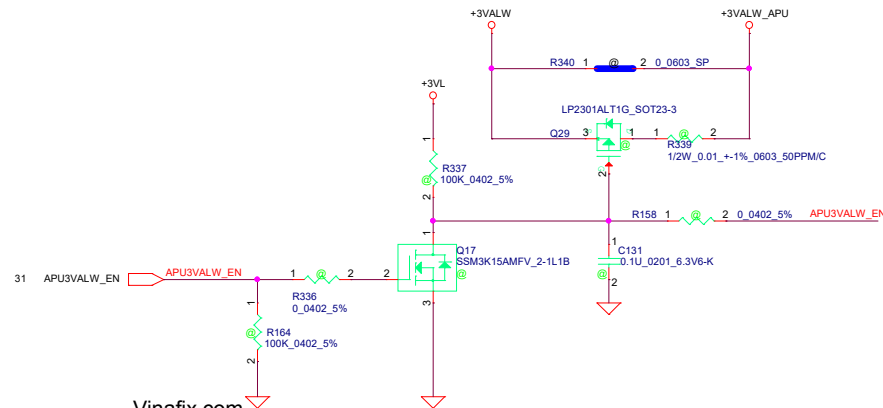
+1.8VALW to +1.8VS



AONS32314
VDS=30V VGS=20V, ID=32A,
Rds=8.7mohm @ VGS=10V
VGS(th)=2.25V Max

20VSB will change to 6V in DC mode, careful the Res divide voltage

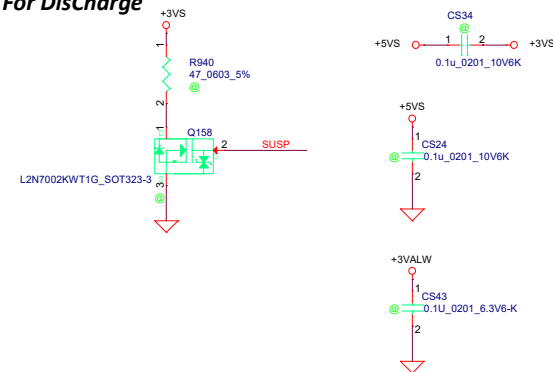
+3VALW to +3VALW_APU



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Disable +3VALW_APU when Mirror code

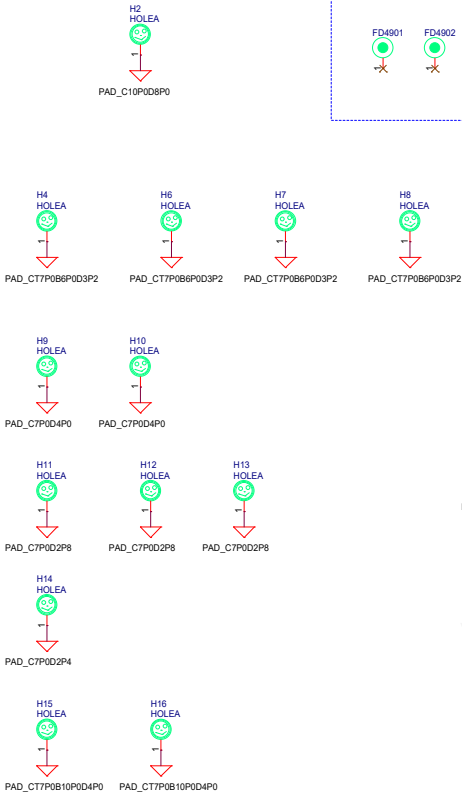
For DisCharge



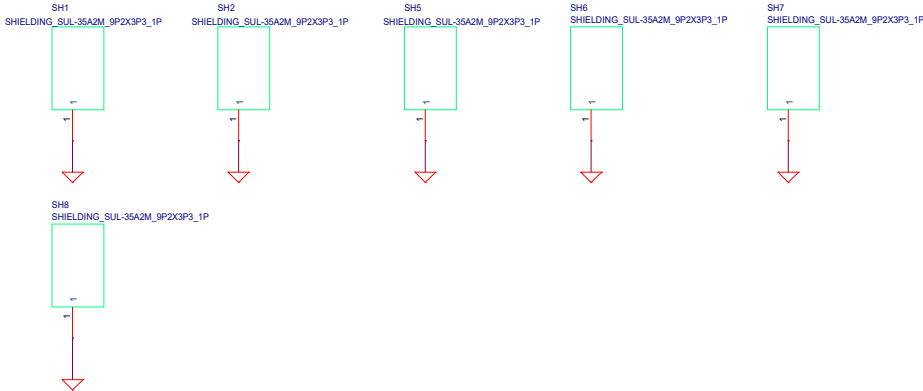
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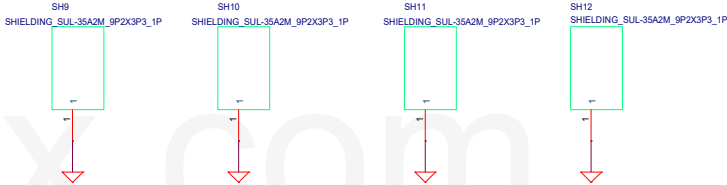
PCB Federal Mark PAD



SO-DIMM Shielding



Memory Down Shielding




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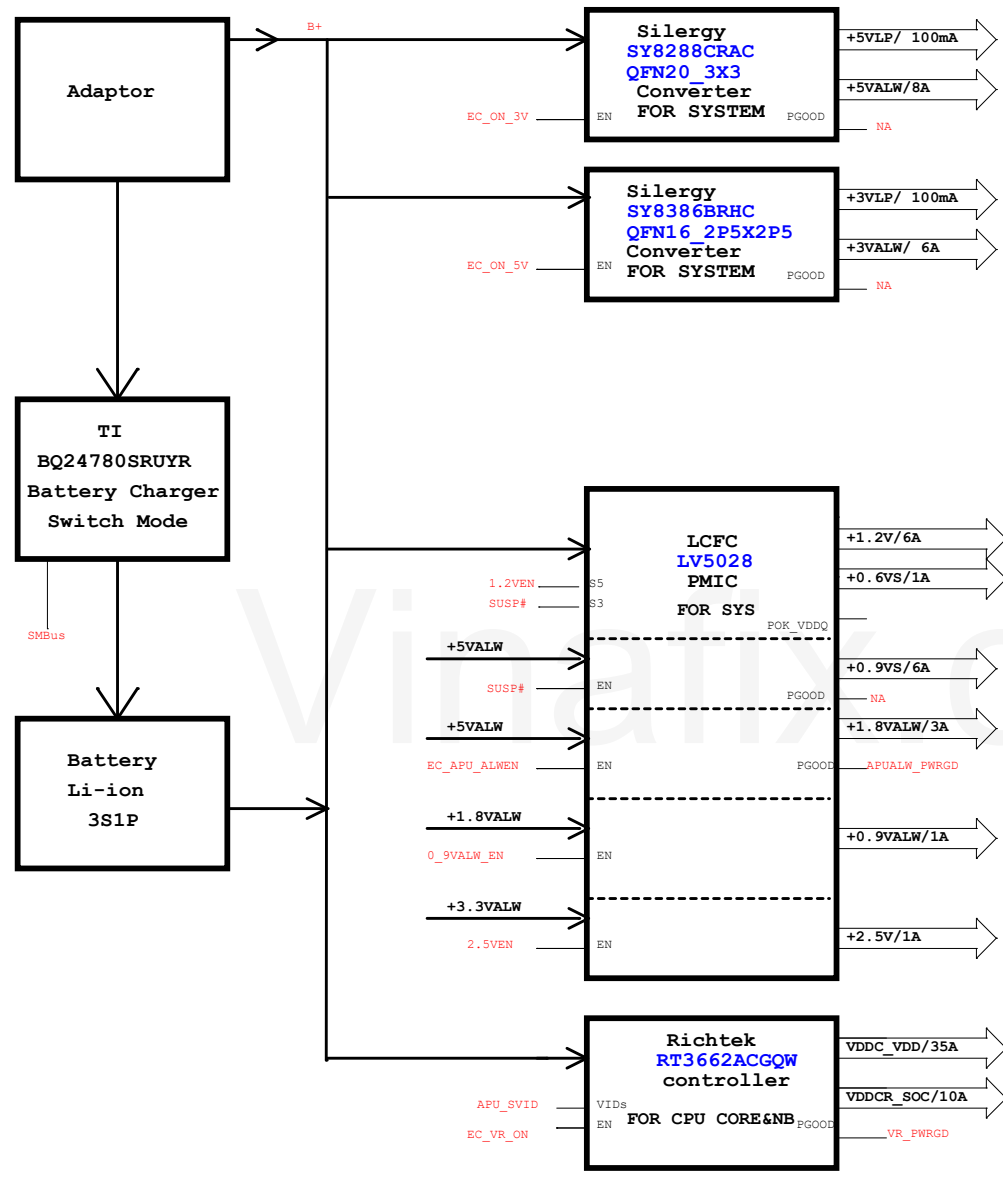
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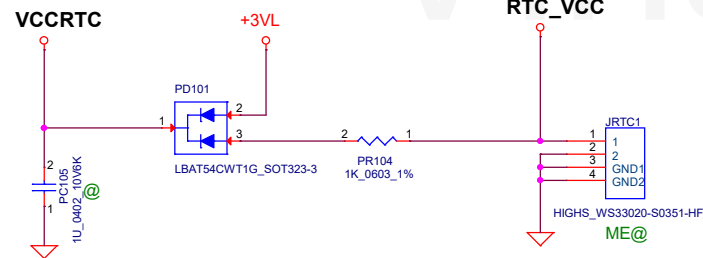
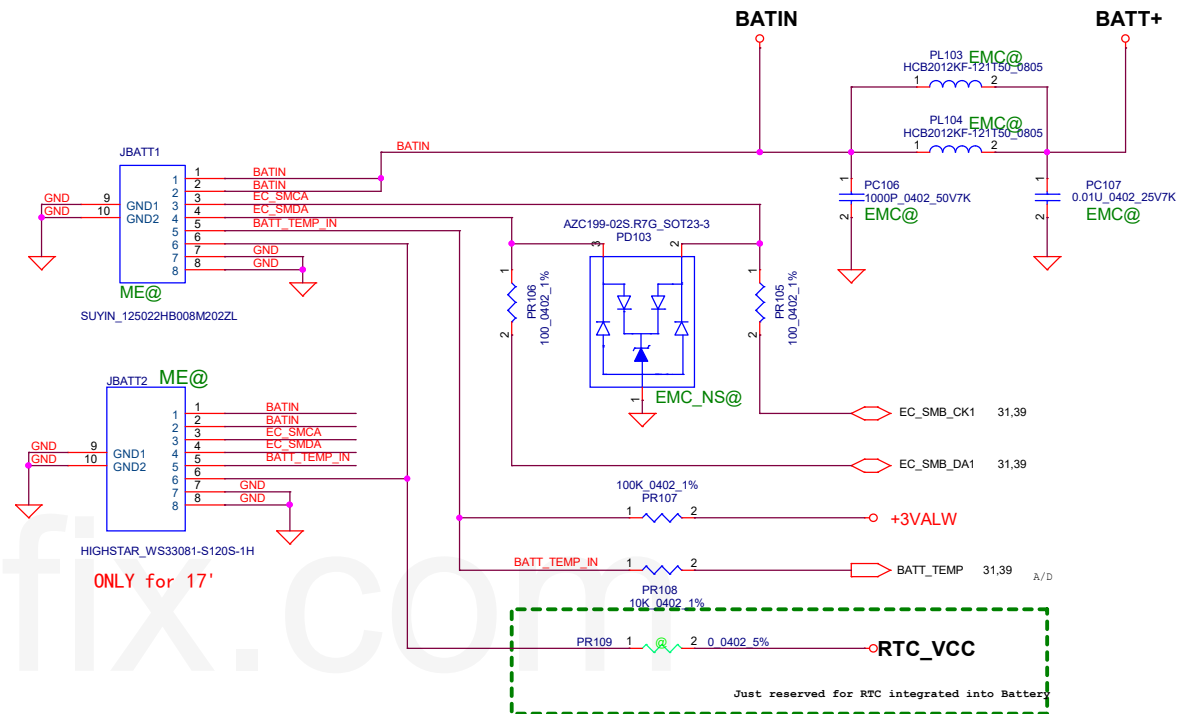
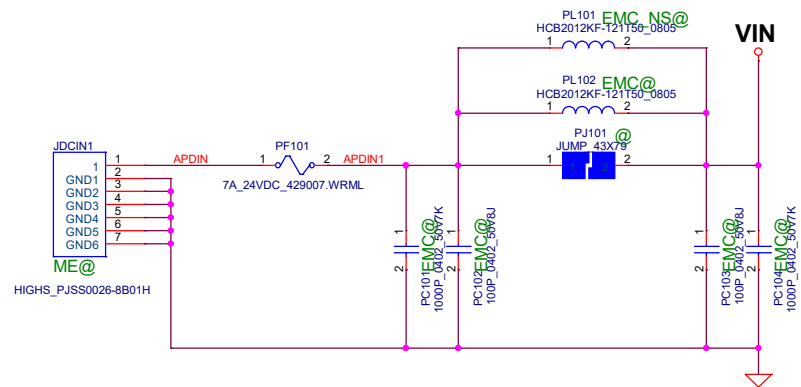
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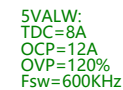
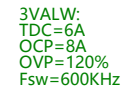
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